

6 in the first directory of an address tag associated with the first memory block;
7 applying the first control signal to a first multiplexer having inputs
8 connected to the cache entry array;
9 constructing a second control signal for the second memory block based
10 on a second location in the second directory of an address tag associated with
11 the second memory block; and
12 applying the second control signal to a second multiplexer having inputs
13 connected to the cache entry array.

1 4. (unchanged) The method of Claim 1 wherein the cache has first and
2 second cache entry arrays, and said step reading the first memory block while
3 reading the second memory block includes the steps of:

4 constructing a first control signal for the first memory block based on a
5 first location in the first directory of an address tag associated with the first
6 memory block;

7 applying the first control signal to a first multiplexer having inputs
8 connected to the first cache entry array;

9 constructing a second control signal for the second memory block based
10 on a second location in the second directory of an address tag associated with
11 the second memory block; and

12 applying the second control signal to a second multiplexer having inputs
13 connected to the second cache entry array.

1 5. (deleted)

1 2
2 6. (amended) The method of Claim [2] 1 wherein each of the first and
3 second cache directories have a plurality of congruence classes each having
4 a plurality of lines for storing the address tags, and said step of the processor
5 reading the first memory block while the system bus is reading the second
6 memory block includes the steps of:

7 associating a first requested address with a first congruence class in the
first cache directory;

8 comparing each of the address tags stored in the first congruence class
9 with a portion of the first requested address;
10 associating a second requested address with a second congruence class
11 in the second cache directory; and
12 comparing each of the address tags stored in the second congruence
13 class with a portion of the second requested address.

1 7. (unchanged) The method of Claim 3 wherein the first cache directory
2 is connected to a first interconnect on a processor side of the cache, and the
3 second cache directory is connected to a second interconnect on a system bus
4 side of the cache, and said step of reading the first memory block while reading
5 the second memory block further includes the steps of:

6 presenting the first memory block to the first interconnect by connecting
7 the first interconnect to an output of the first multiplexer; and

8 presenting the second memory block to the second interconnect by
9 connecting the second interconnect to an output of the second multiplexer.

1 8. (unchanged) The method of Claim 4 wherein the first cache directory
2 is connected to a first interconnect on a processor side of the cache, and the
3 second cache directory is connected to a second interconnect on a system bus
4 side of the cache, and said step of reading the first memory block while reading
5 the second memory block further includes the steps of:

6 presenting the first memory block to the first interconnect by connecting
7 the first interconnect to an output of the first multiplexer; and

8 presenting the second memory block to the second interconnect by
9 connecting the second interconnect to an output of the second multiplexer.

1 9. (unchanged) The method of Claim 6 wherein, if an error occurs when
2 examining a particular address tag as part of said step of comparing the
3 address tags stored in the first congruence class, then a redundant address tag
4 is substituted for the particular address tag by examining a line of the second
5 cache directory which corresponds with the line in the first cache directory
6 containing the particular address tag.

1 8 10. (amended) A computer system comprising:
2 a processor;
3 a memory device;
4 a system bus connected to said memory device;
5 a cache having a plurality of cache lines for storing memory blocks
6 corresponding to addresses of said memory device; [and]
7 means for simultaneously reading a first memory block from said cache
8 and reading a second memory block from said cache in a single clock cycle of
9 said processor, wherein said simultaneous reading means including first and
10 second redundant cache directories; and
11 means for writing an address tag of a memory block which is stored in
12 said cache to a specific line of said first cache directory and to a specific line
13 of said second directory that corresponds to said specific line of said first cache
14 directory.

1 11. (deleted)

1 12. (deleted)

1 13. (deleted)

1 9 14. (amended) The computer system of Claim [11] 8 10 wherein said
2 cache has a single cache entry array, and said simultaneous reading means
3 includes means for:

4 constructing a first control signal for said first memory block based on a
5 first location in said first directory of an address tag associated with said first
6 memory block;

7 applying said first control signal to a first multiplexer having inputs
8 connected to said cache entry array;

9 constructing a second control signal for said second memory block
10 based on a second location in said second directory of an address tag
11 associated with said second memory block; and

12 applying said second control signal to a second multiplexer having inputs
13 connected to said cache entry array.

1 ¹⁰ 15. (amended) The computer system of Claim [11] ⁸ 10 wherein said
2 cache has first and second cache entry arrays, and said simultaneous reading
3 means includes means for:

4 constructing a first control signal for said first memory block based on a
5 first location in said first directory of an address tag associated with said first
6 memory block;

7 applying said first control signal to a first multiplexer having inputs
8 connected to said first cache entry array;

9 constructing a second control signal for said second memory block
10 based on a second location in said second directory of an address tag
11 associated with said second memory block; and

12 applying said second control signal to a second multiplexer having inputs
13 connected to said second cache entry array.

1 ¹¹ 16. (amended) The computer system of Claim [11] ⁸ 10 wherein each of
2 said first and second cache directories have a plurality of congruence classes
3 each having a plurality of lines for storing [said] address tags, and said
4 simultaneous reading means further includes means for:

5 associating a first requested address with a first congruence class in said
6 first cache directory;

7 comparing each of said address tags stored in said first congruence
8 class with a portion of said first requested address;

9 associating a second requested address with a second congruence class
10 in said second cache directory; and

11 comparing each of said address tags stored in said second congruence
12 class with a portion of said second requested address.

1 17. (unchanged) The computer system of Claim 14 further comprising
2 a first interconnect for communicating with said processor, and a second

3 interconnect for communicating with said system bus, and wherein said
4 simultaneous reading means further includes means for:

5 presenting said first memory block to said first interconnect by
6 connecting said first interconnect to an output of said first multiplexer; and

7 presenting said second memory block to said second interconnect by
8 connecting said second interconnect to an output of said second multiplexer.

1 18. (unchanged) The computer system of Claim 15 further comprising
2 a first interconnect for communicating with said processor, and a second
3 interconnect for communicating with said system bus, and wherein said
4 simultaneous reading means further includes means for:

5 presenting said first memory block to said first interconnect by
6 connecting said first interconnect to an output of said first multiplexer; and

7 presenting said second memory block to said second interconnect by
8 connecting said second interconnect to an output of said second multiplexer.

1 19. (unchanged) The computer system of Claim 16 wherein, if an error
2 occurs when examining a particular address tag as part of said comparing of
3 said address tags stored in said first congruence class, then a redundant
4 address tag is substituted for said particular address tag by examining a line
5 of said second cache directory which corresponds with a line in said first cache
6 directory containing said particular address tag.--